

Figure 1

PRIOR ART

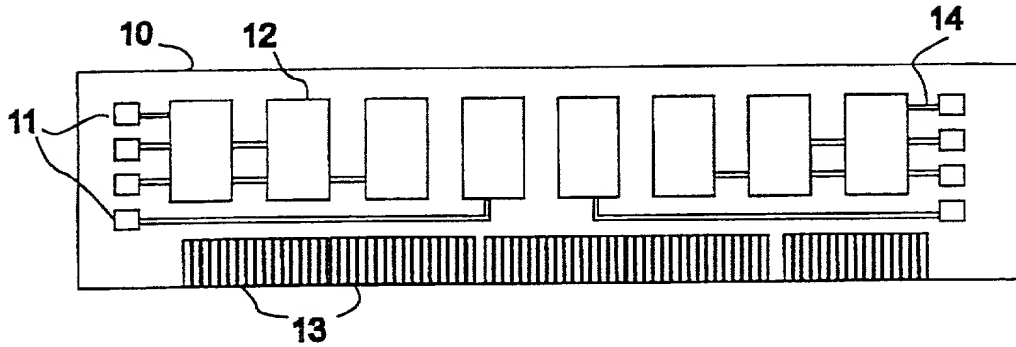


Figure 2

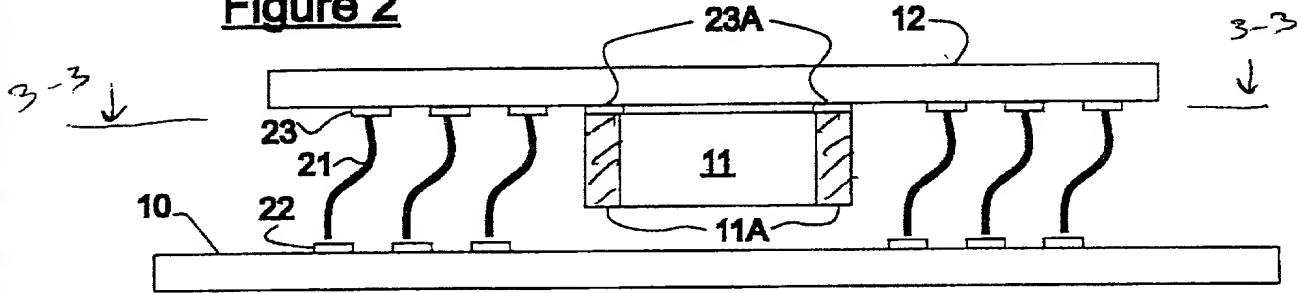


Figure 3

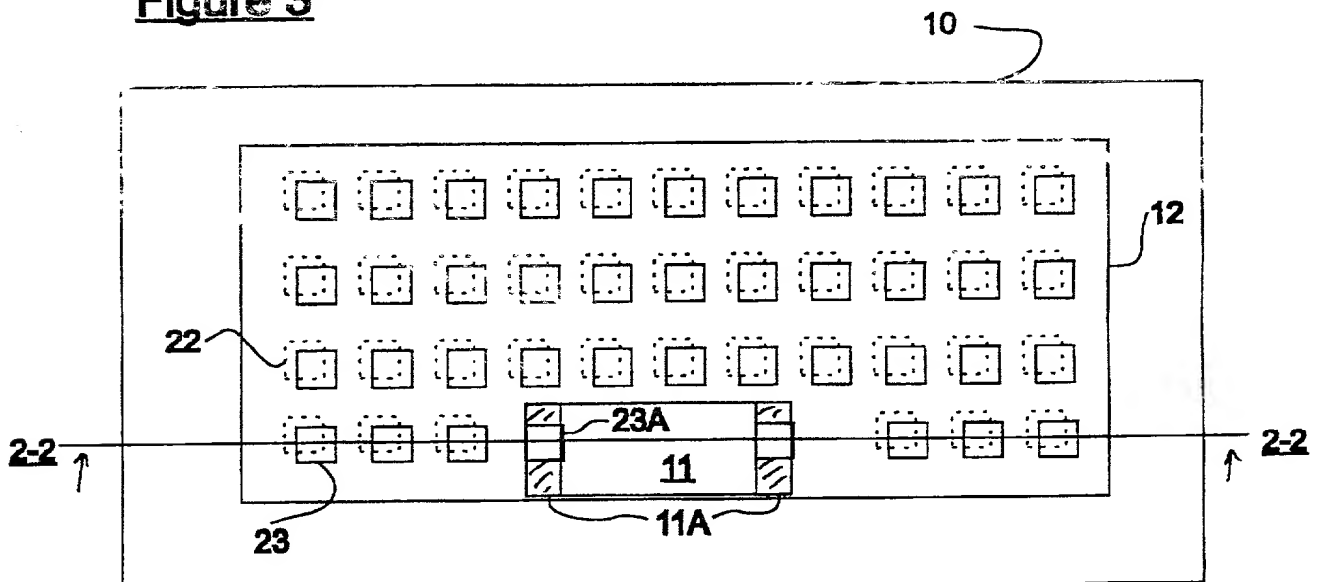


Figure 4A

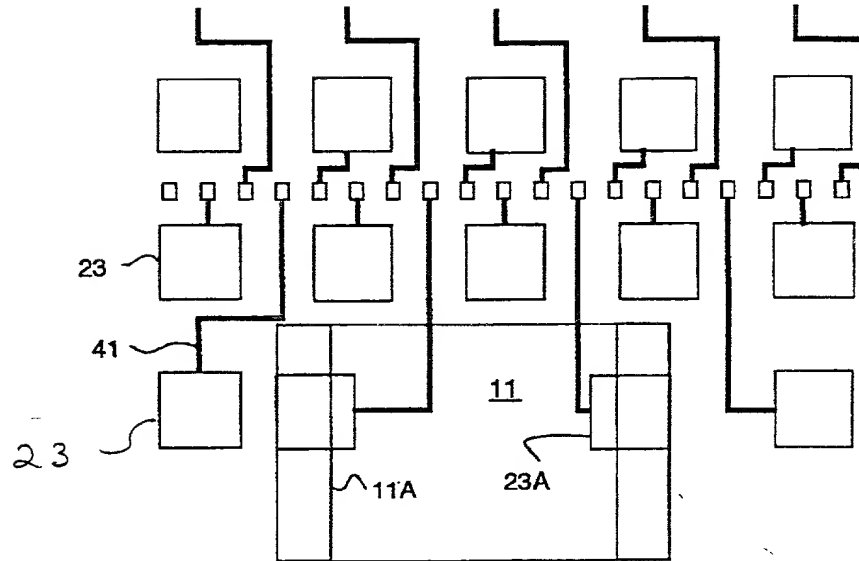


Figure 7A

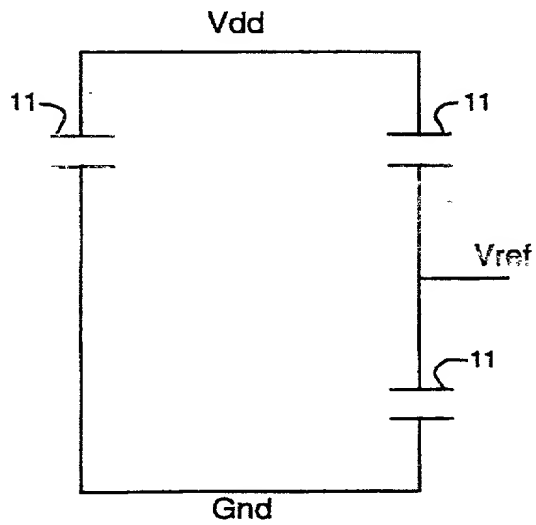


Figure 7B

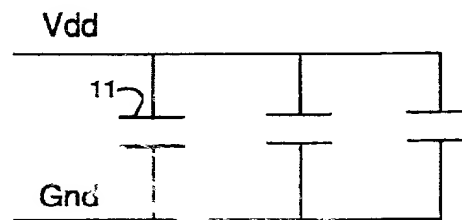


Figure 4B

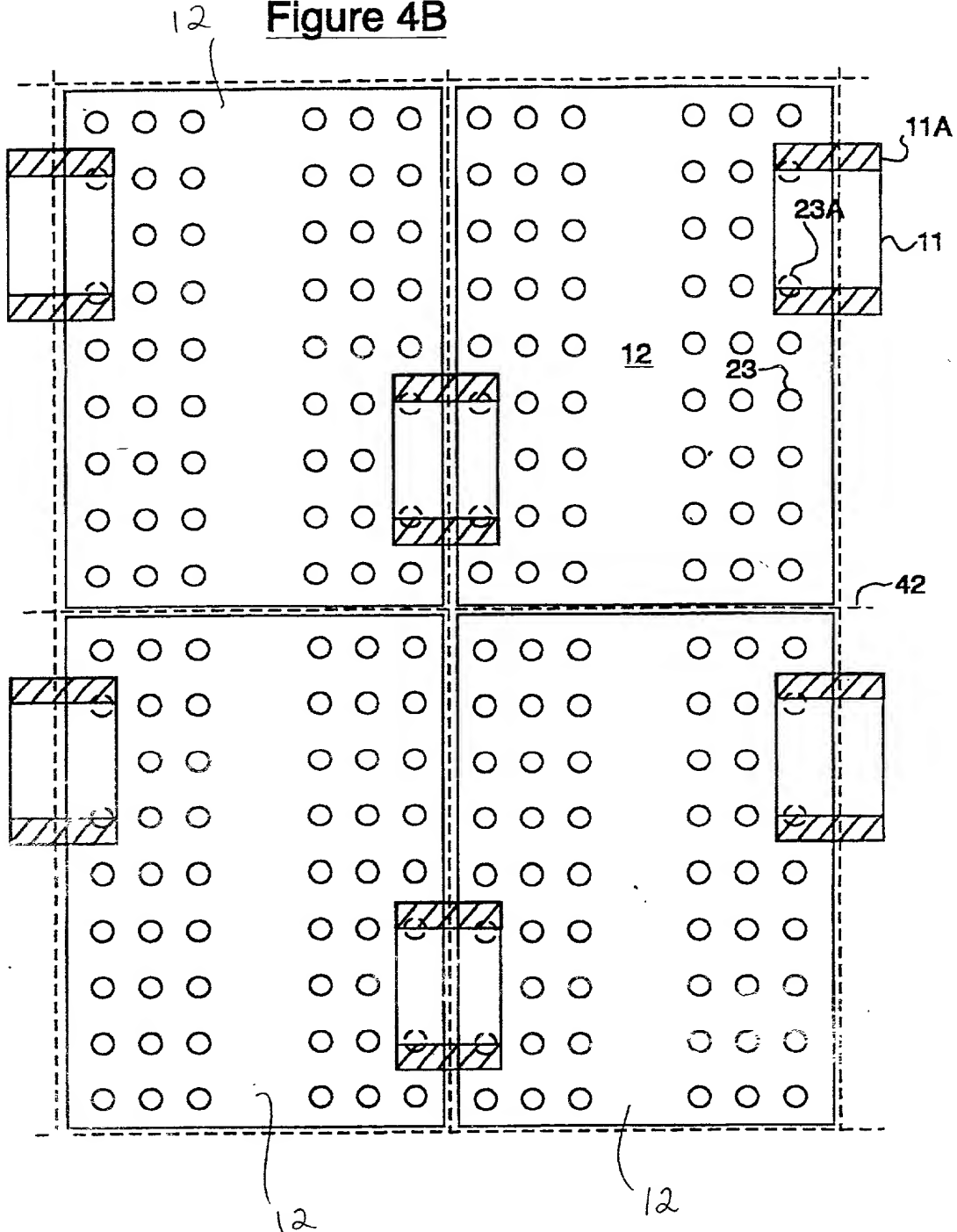


Figure 5

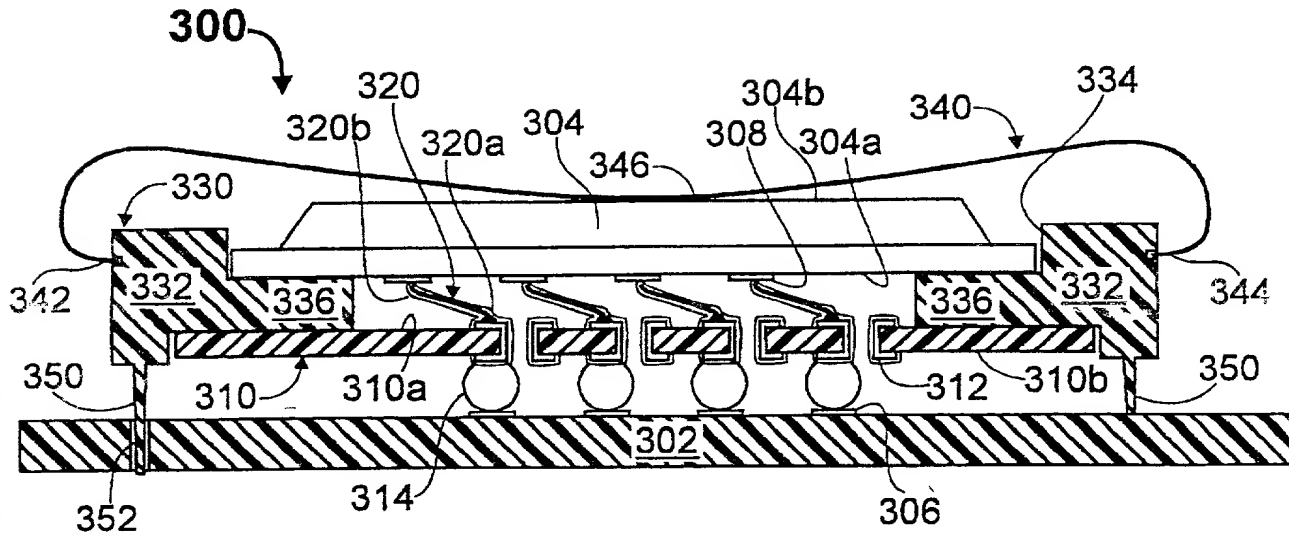


Figure 6

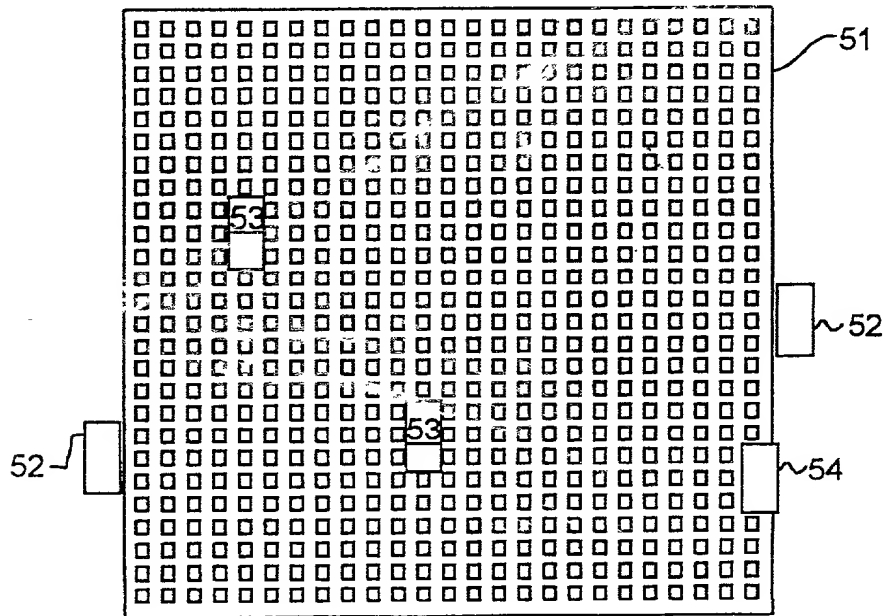


Fig. 8A

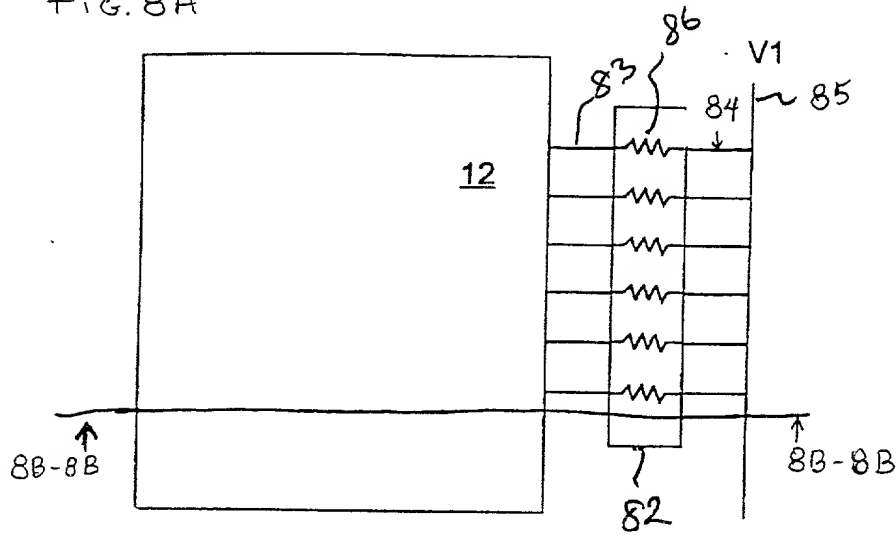


Figure 8B

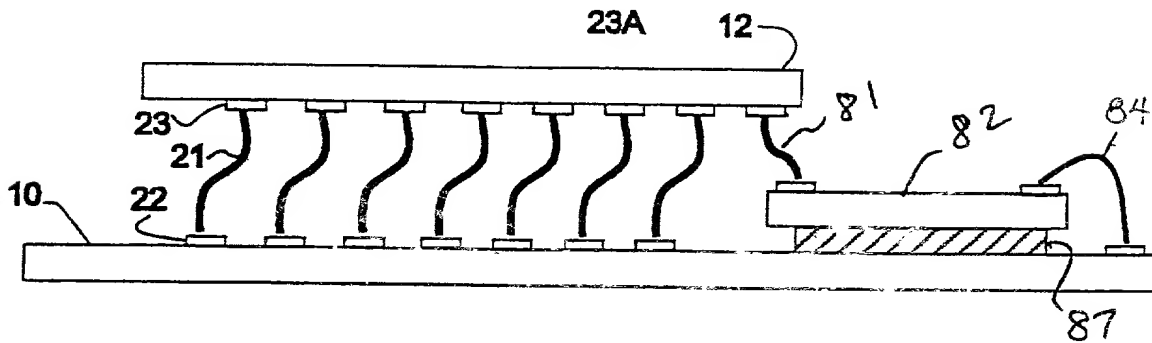


FIG. 9A

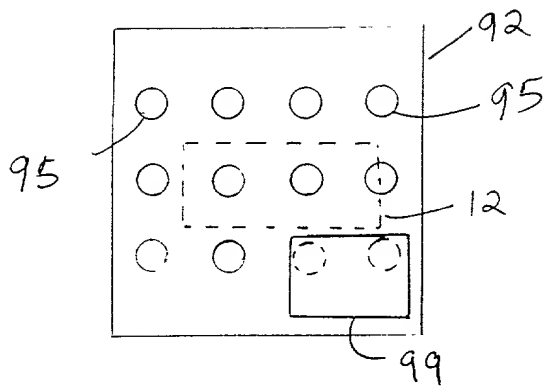


FIG. 9B

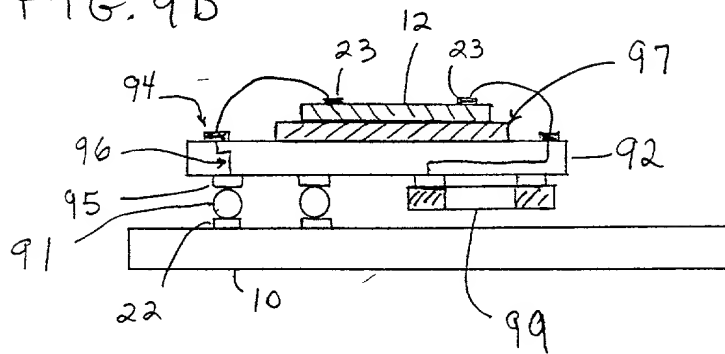


FIG. 10

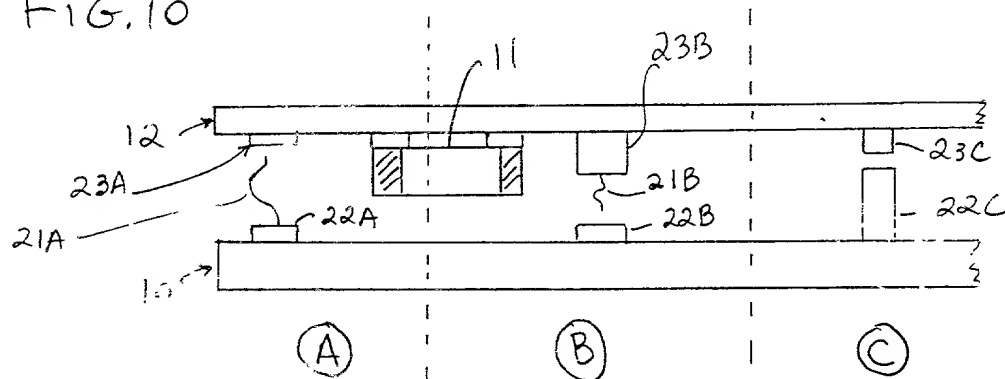


Figure 11
 (Prior Art)

500

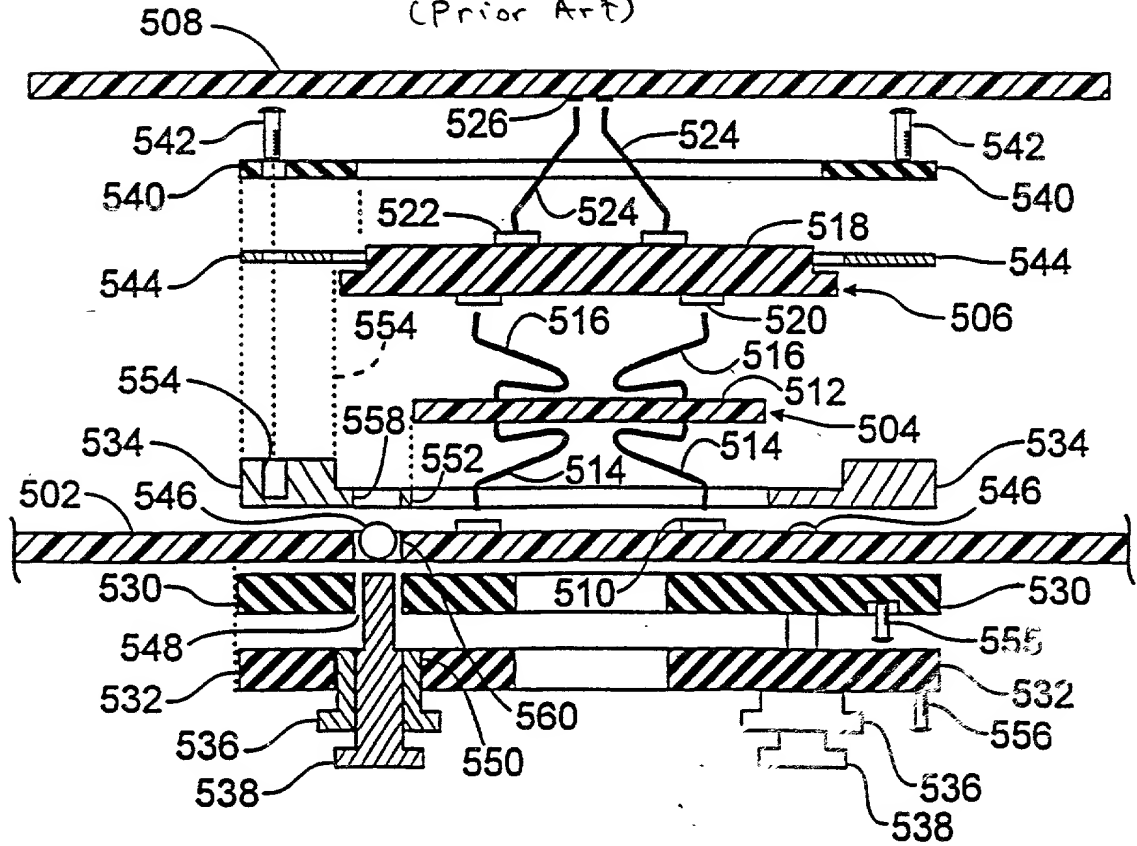


Figure 12 A
(Prior Art)

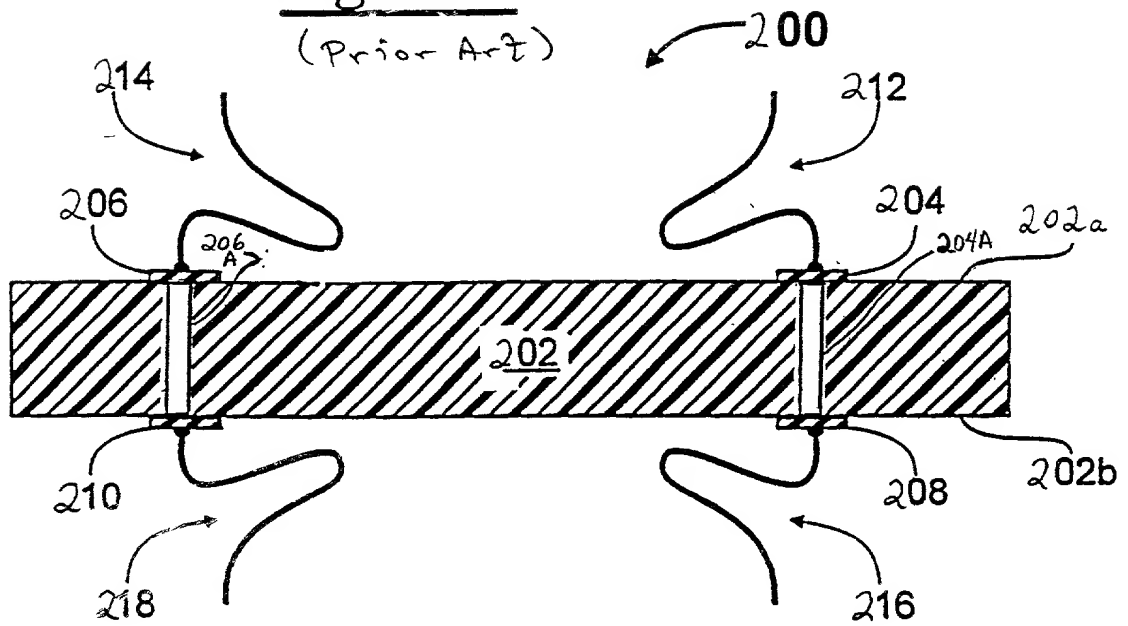


FIG. 12A

FIG. 12B (Prior Art)

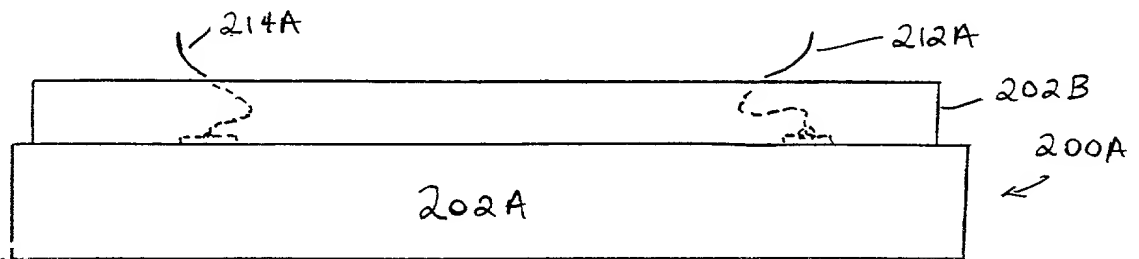


FIG. 12C (Prior Art)

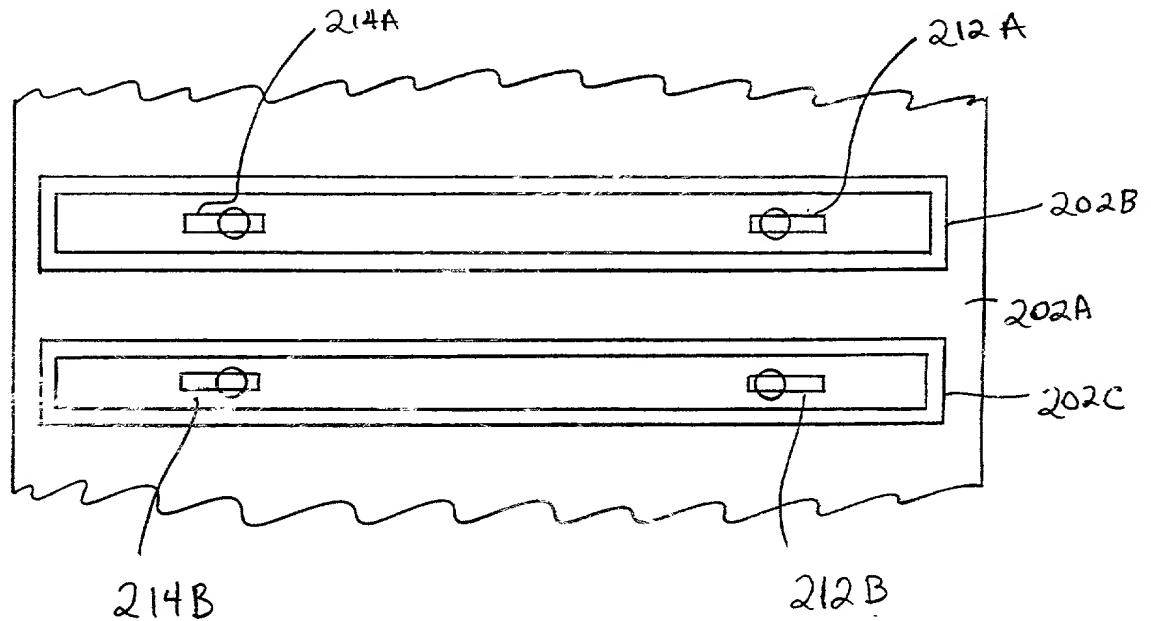


Figure 13 A (Prior Art)

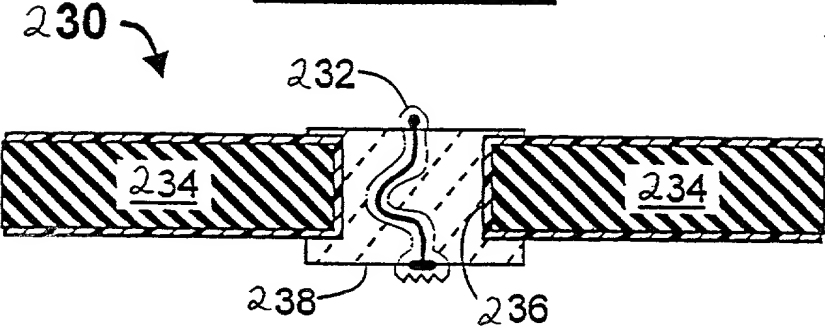


Figure 13 B (Prior Art)

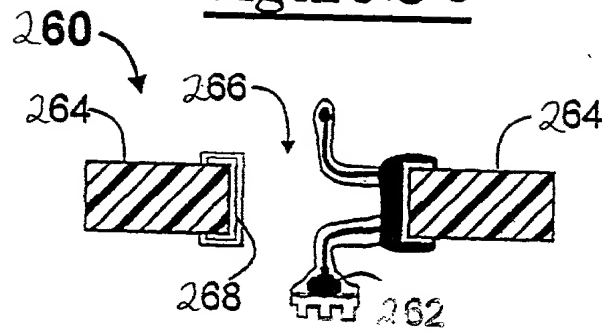
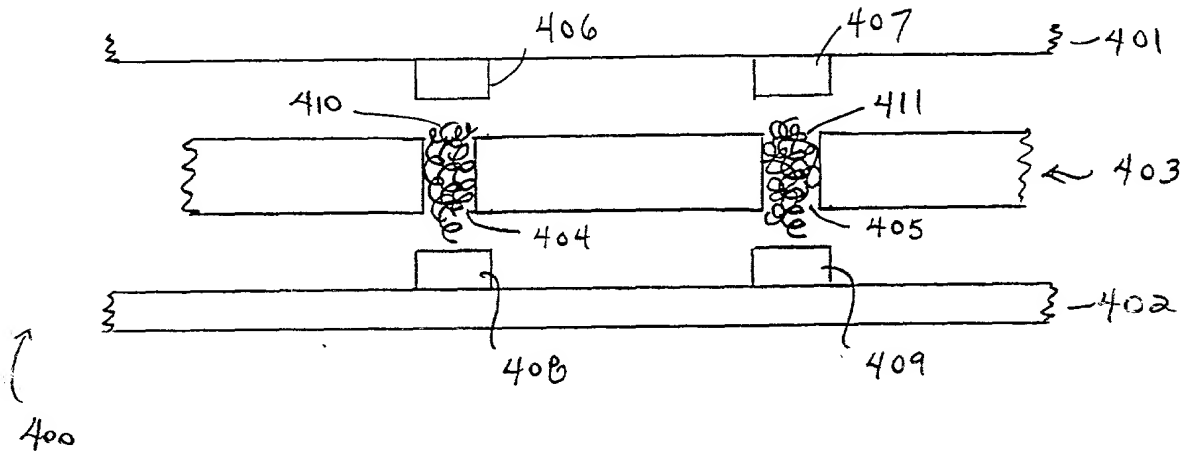


FIG. 14 (Prior Art)



400 403 406 407 408 409 410 411

Figure 15A

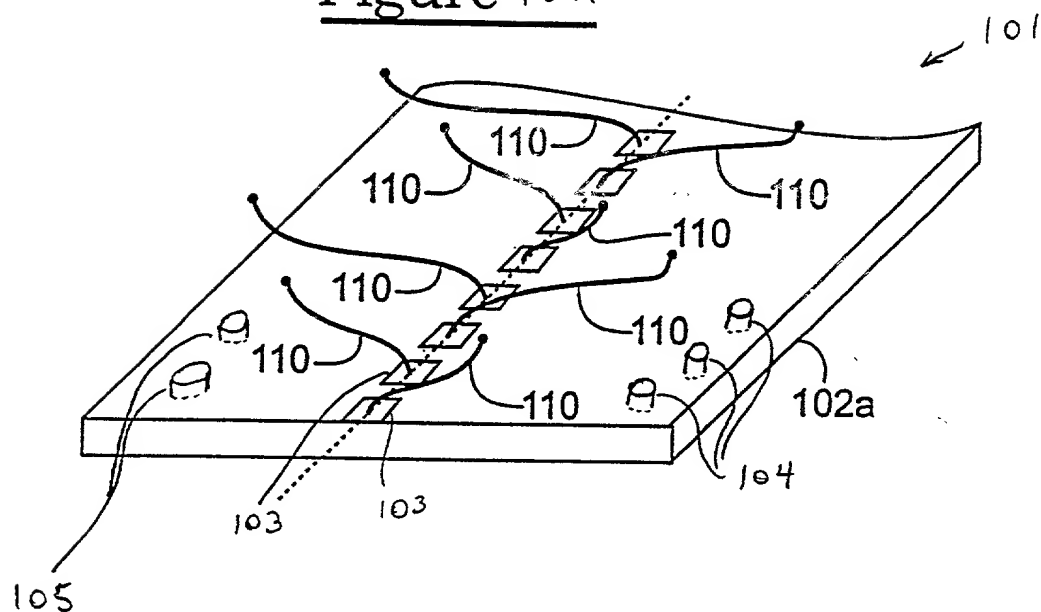


FIG. 15B

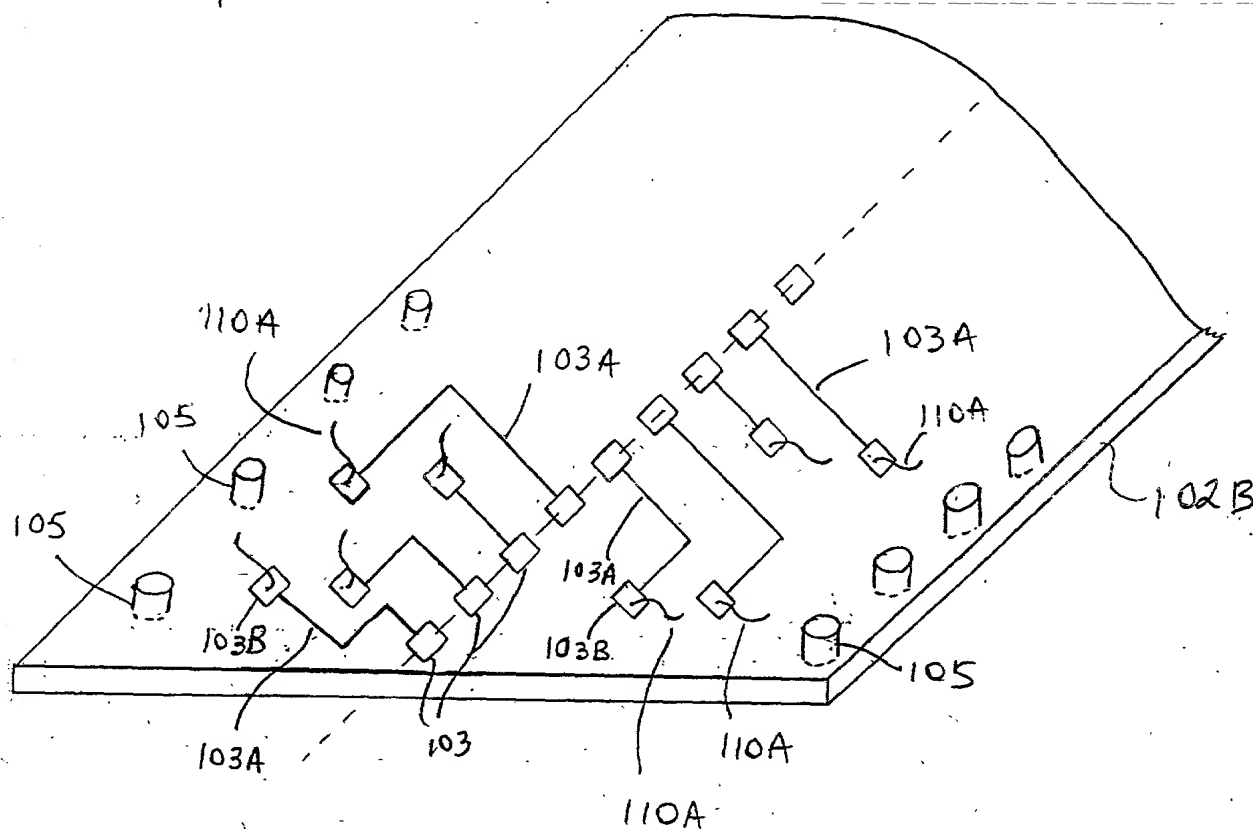


FIG. 16 A

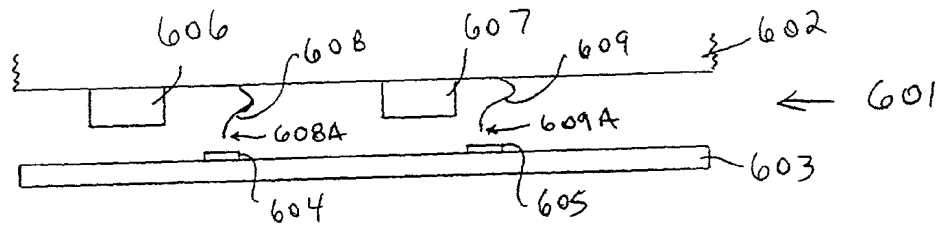


FIG. 16 B

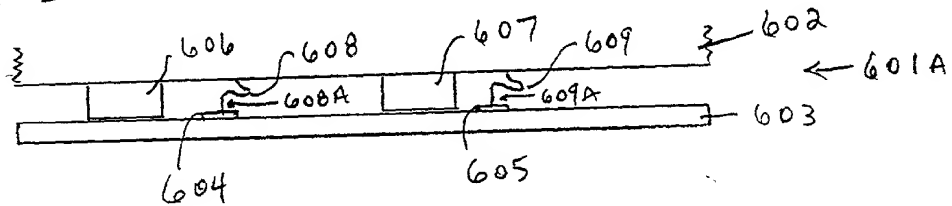


FIG. 17

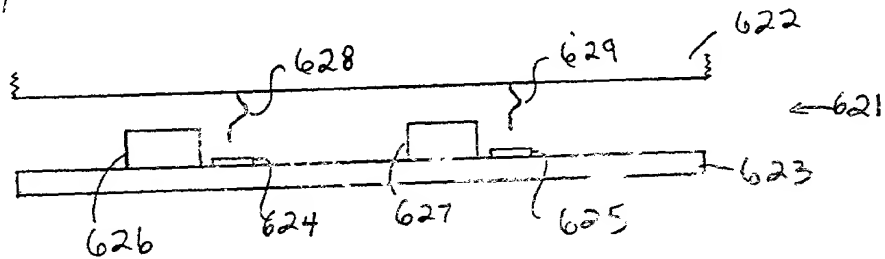


FIG. 16C

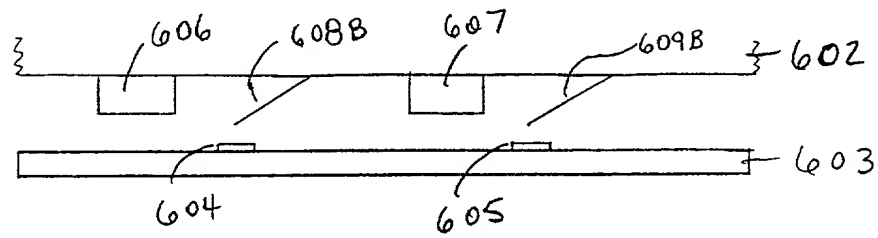


FIG. 16D

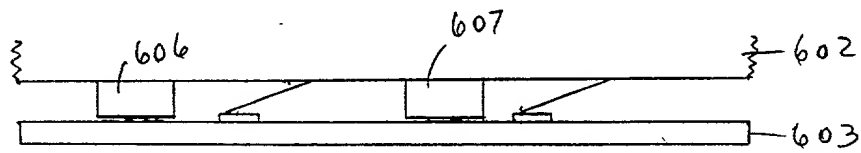


FIG. 18 A

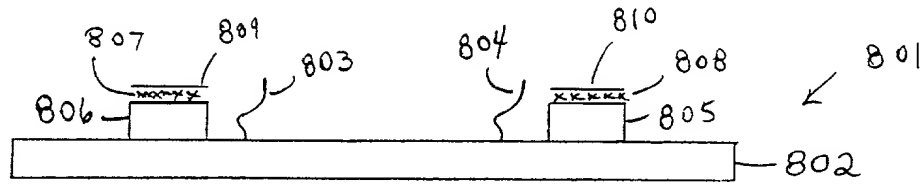
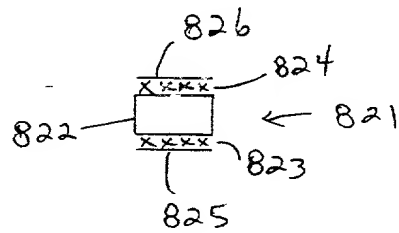


FIG. 18 B



A cross-sectional view of a semiconductor device 1401. The device is built on a substrate 1402. A gate stack 1403 is formed on the substrate, with a gate dielectric layer 1403A. The gate stack is divided into two regions by a trench 1404. The left region contains a gate stack 1421, which is connected to a source region 1423 and a drain region 1425. The right region contains a gate stack 1411, which is connected to a source region 1413 and a drain region 1415. The source regions are connected to a common source line 1405, which is connected to a voltage source V_{SS} . The drain regions are connected to a common drain line 1406, which is connected to a voltage source V_{DD} . The substrate 1402 is shown with a cross-section line 1403A.